What is claimed is:

1. A current regulation circuit, comprising:

a current mirror arranged with a sense transistor and a power transistor;

a current sink that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit; and

a control component that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor.

2. The circuit of Claim 1, further comprising a component that outputs a signal if the drain voltage of the sense resistor is substantially equivalent to the drain voltage of the power transistor.

3. The circuit of Claim 2, wherein the component is at least one of a comparator and a differential amplifier.

4. The circuit of Claim 2, wherein the control component employs the signal to substantially turn off the current flowing through the power transistor.

5. The circuit of Claim 2, wherein the control component employs the signal to modulate the amount of current flowing through the power transistor to be less than the limit.

6. The circuit of Claim 1, wherein the control component senses a feedback signal provided by a load coupled to a drain of the power amplifier, wherein the feedback signal is employed in the control of the operation of the control component.

7. The circuit of Claim 1, wherein the current mirror of the power transistor and the sense resistor employs a ratio of m:1.

8. The circuit of Claim 1, wherein the sense resistor and the power transistor are at least field effect transistors (FET).

9. The circuit of Claim 1, further comprises a clock signal that enables the regulation of a switching current flowing through the power transistor.

10. The circuit of Claim 9, further comprising a first switch and a second switch for controlling a switching current that flows through the power transistor, wherein the first switch enables an output of the control component to be coupled to at least the power transistor and the sense transistor and wherein the second switch enables an output from a comparison component to be coupled to the control component, and wherein the comparison component's output indicates if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor.

11. The circuit of Claim 10, wherein the first switch is arranged in an open state and the second switch is arranged in an open state if the switching current flowing through the power transistor and another switching current flowing through the sense resistor are both substantially equivalent to zero.

12. A current regulator, comprising:

a current mirror arranged with a sense transistor and a power transistor;

a current sink that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit;

a control component that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor; and

a comparison component that presents a signal if the drain voltage of the sense resistor is substantially equivalent to the drain voltage of the power transistor.

13. The current regulator of Claim 12, further comprises a clock signal that enables the regulation of a switching current flowing through the power transistor.

14. The current regulator of Claim 12, further comprising a first switch and a second switch for operating with a switching current flowing through the power transistor, wherein the first switch enables an output of the control component to be coupled to at least the power transistor and the sense transistor and wherein the second switch enables signal presented by the comparison component to be coupled to the control component, and wherein the comparison component's signal indicates if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor.

15. The current regulator of Claim 14, wherein the first switch is arranged in an open state and the second switch is arranged in an open state if the switching current flowing through the power transistor and another switching current flowing through the sense resistor are both substantially equivalent to zero.

16. The current regulator of Claim 12, wherein the current flowing through the power transistor is substantially continuous.

17. A current regulation circuit, comprising:

a means for mirroring current flowing in a sense transistor and a power transistor;

a means for sinking current that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense resistor if a current flowing through the power transistor is less than a limit;

a means for limiting the current flowing through the power transistor if the drain voltage of the sense resistor is substantially equivalent to a drain voltage of the power transistor; and

a means for presenting a signal if the drain voltage of the sense resistor is substantially equivalent to the drain voltage of the power transistor.